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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,643	PARK, JONG BUM	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☒ Claim(s) *12 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 have been considered.

Drawings

2. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated instead of the current label, "CONVENTIONAL ART". See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

4. Claims 12 and 17 are objected to because of the following informalities:

   a. Referring to claim 12, please correct line 15 from "arithmetic unit if the condition that the condition is not satisfied, after determining" to read --arithmetic unit if the condition ~~that the condition~~ is not satisfied, after determining—

   b. Referring to claim 17, please correct line 12 from "state information of the state information of the main instruction decoder and main" to read --state information of ~~the state information of~~ the main instruction decoder and main--

5. The Examiner encourages Applicant and/or Applicant's representative to review the claims to ensure other grammatical and word usage mistakes are present. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 2 recites the limitation "the above condition" in line 15. There is insufficient antecedent basis for this limitation in the claim. There has been no previous occurrence of a condition.

8. Claim 4 recites the limitation "the data" in line 6. There is insufficient antecedent basis for this limitation in the claim. There is no occurrence of "data" in previous lines, only "instruction data"

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-2, 4-6, 9-14, and 16-17 are rejected under 35 U.S.C. 102(b) as being taught by Kimura et al., U.S. Patent Number 5,511,172 (herein referred to as Kimura).

11. Referring to claim 1, Kimura has taught a Single Instruction Multiple Data (SIMD) digital signal processor, comprising:

a. An on-chip program memory for storing an instruction data of a program (Kimura column 6, line 64 to column 7, line 30 and Figure 1);

b. A plurality of main instruction decoders for decoding the instruction data and outputting a decoded signal (Kimura column 3, lines 19-30; column 6, line 64 to

column 7, line 9; column 7, lines 36-39; and Figure 1);

c. An on-chip data memory for storing data (Kimura column 6, line 64 to column 7, line 9; column 7, line 66 to column 8, line 12; column 8, lines 39-40; and Figure 1); and

d. A plurality of arithmetic units for calculating the data according to the decoding signal (Kimura column 6, line 64 to column 7, line 9; column 7, lines 40-46; and Figure 1).

12. Referring to claim 2, Kimura has taught wherein the plurality of instruction decoders comprise:

a. A main instruction_decoder for decoding an instruction data performed in case above condition is satisfied, according to the condition of the conditional branch (Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 36-39; and Figure 1); and

b. A sub instruction decoder for decoding an instruction data performed incase the above condition is not satisfied(Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 36-39; and Figure 1).

13. In regards to Kimura, the plurality of decoders inherently function in this manner or else the instructions for both branches of a conditional branch cannot be issued to the instruction units in parallel as disclosed in column5, lines 9-21 of Kimura.

14. Referring to claim 4, Kimura has taught a Single Instruction Multiple Data (SIMD) digital signal processor, comprising:

a. An on-chip program memory for storing an instruction data of a program (Kimura column 6, line 64 to column 7, line 30 and Figure 1);

b. A main instruction decoder for decoding the instruction data and outputting a decoded signal(Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 36-39; and Figure 1);

c. A sub instruction decoder for decoding a received instruction data in case of an instruction mode related to a conditional branch (Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 36-39; and Figure 1);

d. An on-chip data memory for storing the data (Kimura column 6, line 64 to column 7, line 9; column 7, line 66 to column 8, line 12; column 8, lines 39-40; and Figure 1);.

e. A main arithmetic unit for calculating the data according to the decoded signal of the main instruction decoder (Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 40-46; column 8, line 66 to column 8, line 12; and Figure 1); and

f. A sub arithmetic unit for calculating the data identically as the main arithmetic unit according to the decoded signal of the main instruction decoder or calculating the data according to the decoded signal of the sub instruction decoder (Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 40-46; column 8, line 66 to column 8, line 12; and Figure 1).

15. In regards to Kimura, the plurality of decoders inherently function in this manner or else the instructions for both branches of a conditional branch cannot be issued to the instruction units in parallel as disclosed in column5, lines 9-21 of Kimura.

16. Regarding claim 5, Kimura has taught an arithmetic method for a Single Instruction Multiple Data (SIMD) digital signal processor, comprising the steps of:

a. Decoding an instruction data fetched from an on-chip program memory in the main instruction decoder (Kimura column 3, lines 19-30; column 6, line 64 to column 7, line 9; column 7, lines 36-39; and Figure 1); and

b. Calculating according to the characteristic of the instruction data after determining the characteristic of the decoded instruction data (Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 40-46; column 8, line 66 to column 8, line 12; and Figure 1).

17. Referring to claim 6, Kimura has taught

a. Transmitting the decoded instruction data into a main arithmetic unit in case the characteristic of the instruction data corresponds to the normal instruction data in

the result of the above determination (Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 36-39; and Figure 1); and

b. Calculating in the main arithmetic unit, according to the decoded instruction data by reading a data necessary for calculating from the on-chip data (Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 40-46; column 8, line 66 to column 8, line 12; and Figure 1).

18. Referring to claim 9, Kimura has taught

a. Calculating according to the decoded instruction data in case the characteristic of the instruction data corresponds to a predetermined conditional branch in the result of the above determination (Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 40-46; column 8, line 66 to column 8, line 12; and Figure 1); and

b. Respectively decoding the instruction data by fetching simultaneously the instruction data which will be performed in case the condition of the conditional branch is satisfied and in case not satisfied calculating according to the decoded instruction data (Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 36-39; and Figure 1).

19. Referring to claim 10, Kimura has taught

a. Decoding the instruction data by fetching the instruction data which will be performed in case the condition of the conditional branch is satisfied and decoding in the sub instruction decoder by fetching the instruction data which will be performed in case the condition of the conditional branch, at the same time (Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 36-39; and Figure 1); and

b. Calculating the in the main arithmetic unit and sub arithmetic unit respectively, according to the decoded instruction data by reading a data necessary for calculating from the on-chip data memory (Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 40-46; column 8, line 66 to column 8, line 12; and Figure 1).

20. Referring to claim 11, Kimura has taught maintaining the state information of the main instruction decoder and main arithmetic unit if the condition that the condition is satisfied, after determining the condition of the conditional branch, and deleting the state information of the sub-instruction decoder and sub arithmetic unit (Kimura column 1, line 55 to column 2, line 40; column 4, lines 5-27; column 5, lines 9-20; column 7, line 66 to column 8, line 12; and Figure 1).

21. Referring to claim 12, Kimura has taught deleting the state information of the main instruction decoder and main arithmetic unit if the condition is not satisfied, after determining the condition of the conditional branch, and replacing the information with the state information of the sub instruction decoder and sub arithmetic unit (Kimura column 1, line 55 to column 2,

line 40; column 4, lines 5-27; column 5, lines 9-20; column 7, line 66 to column 8, line 12; and Figure 1).

22. Referring to claim 13, Kimura has taught an arithmetic method for a Single Instruction Multiple Data (SIMD) digital signal processor, comprising the steps of:

a. Determining the characteristic of the decoded instruction data by decoding the instruction data fetched from the on-chip program memory in the main instruction decoder (Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 36-39; and Figure 1);

b. Transmitting the decoded instruction data into the main arithmetic unit in case the characteristic of the instruction data corresponds to a predetermined conditional branch in the result of the above determination (Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 36-39; and Figure 1);

c. Calculating the condition of the conditional branch in the main arithmetic unit according to the decoded instruction data by reading the data necessary for calculating from an on-chip data memory (Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 40-46; column 8, line 66 to column 8, line 12; and Figure 1);

d. Decoding the instruction data respectively in the main instruction decoder and sub

instruction decoder by simultaneously fetching the instruction data which will be performed in case the condition of the conditional branch is satisfied and in case not satisfied and then calculating respectively in the main arithmetic unit and sub arithmetic unit according to the decoded instruction data (Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 36-39; and Figure 1); and

e. Deleting one among the state information of the main instruction decoder and main arithmetic unit and the state information of the sub instruction decoder and sub arithmetic unit, according to the satisfaction of the condition, when the condition of the conditional branch is determined (Kimura column 1, line 55 to column 2, line 40; column 4, lines 5-27; column 5, lines 9-20; column 7, line 66 to column 8, line 12; and Figure 1). In regards to Kimura, the wrong speculative data is essentially deleted since it, essentially, does not exist to the system anymore and the memory it was stored in can be used for something else.

23. Referring to claim 14, Kimura has taught

a. Transmitting the decoded instruction data into a main arithmetic unit in case the characteristic of the instruction data corresponds to the normal instruction data in the result of the above determination (Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 36-39; and Figure 1); and

b. Calculating in the main arithmetic unit, according to the decoded instruction data by reading a data necessary for calculating from the on-chip data (Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 40-46; column 8, line 66 to column 8, line 12; and Figure 1).

24. Referring to claim 16, Kimura has taught wherein the condition is satisfied, the state information of the main instruction decoder and main arithmetic unit is left as it is and the state information of the sub instruction decoder and sub arithmetic unit is deleted (Kimura column 1, line 55 to column 2, line 40; column 4, lines 5-27; column 5, lines 9-20; column 7, line 66 to column 8, line 12; and Figure 1).

25. Referring to claim 17, Kimura has taught wherein the condition is not satisfied, the state information of the main instruction decoder and main arithmetic unit is deleted and the information is replaced by the state information of the sub instruction decoder and sub arithmetic unit (Kimura column 1, line 55 to column 2, line 40; column 4, lines 5-27; column 5, lines 9-20; column 7, line 66 to column 8, line 12; and Figure 1).

Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claims 3, 7-8, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al., U.S. Patent Number 5,511,172 (herein referred to as Kimura) in view of Lecture 29 ©11 August 2000 (herein referred to as Lec29). Kimura has taught

a. Wherein the plurality of arithmetic units independently calculate according to the characteristic of the instruction data (Applicant's claim 3) (Kimura column 6, line 64 to column 7, line 9; column 7, lines 40-46; and Figure 1).

b. Transmitting the decoded instruction data into a main arithmetic unit and sub arithmetic unit in case the characteristic of the instruction data corresponds to the instruction data in the result of the above determination (Applicant's claims 7 and 15) (Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 40-46; column 8, line 66 to column 8, line 12; and Figure 1); and

c. Calculating in the main arithmetic unit and sub arithmetic unit respectively, according to the decoded instruction data by reading a data necessary for calculating from the on-chip data memory (Applicant's claims 7 and 15) (Kimura column 1, line 31 to column 2, line 41; column 3, lines 19-30; column 4, lines 5-27; column 5, lines 10-20; column 6, line 64 to column 7, line 9; column 7, lines 40-46; column 8, line 66 to column 8, line 12; and Figure 1).

28. Kimura has not explicitly taught

a. Wherein the plurality of arithmetic units identically calculate according to the characteristic of the instruction data (Applicant's claim 3);

b. SIMD instruction data (Applicant's claims 7 and 15); and

c. Wherein the calculations in the main arithmetic unit and sub arithmetic unit are identical (Applicant's claim 8).

29. However, Kimura has taught parallel processing (Kimura column 1, lines 31-50) and execution units that execute the same type of instructions (Kimura column 7, lines 40-46 and Figure 1). Lec29 has taught

a. Wherein the plurality of arithmetic units identically calculate according to the characteristic of the instruction data (Applicant's claim 3);

b. SIMD instruction data (Applicant's claims 7 and 15); and

c. Wherein the calculations in the main arithmetic unit and sub arithmetic unit are identical (Applicant's claim 8).

30. A person of ordinary skill in the art at the time the invention was made would have recognized a SIMD device is a parallel processing system that executes a single instruction on multiple data, i.e. perform the same instruction in multiple execution units, simultaneously (Lec29 page 9, paragraph 5 to page 10, paragraph 2), thereby decreasing the amount of time needed to perform the same instruction on large amounts of data, such as in graphics processors. This, in turn, increases the processing speed of the system, since the time to complete large repetitive tasks decreases. Therefore, it would have been obvious to person of ordinary skill in the art at the time the invention was made to incorporate the SIMD instructions of Lec29 in the device of Kimura to increase processing speed.

Conclusion

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Wilkinson et al., U.S. Patent Number 5,805,915, has taught a SIMD system that can execute in MIMD mode, i.e. different instructions on multiple data, in certain conditions to eliminate performance inhibitors, such as conditional branches.

b. Sharangpani et al., U.S. Patent Number 5,860,017 and 6,065,115, has taught a system which fetches and executes both branch paths.

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

33. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

34. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
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1 November 2004

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